3. A Wave Dynamic Differential Logic, comprising:

a differential logic cell having inverted combinatorial data-bearing inputs and corresponding non-inverted combinatorial data-bearing inputs, said differential logic cell configured to provide one or more inverted logic outputs and corresponding one or more non-inverted logic outputs, said differential logic cell configured to receive a precharge wave and/or a predischarge wave on said inverted combinatorial data-bearing inputs and non-inverted combinatorial data-bearing inputs and to propagate said precharge wave and/or said predischarge wave from said inverted combinatorial data-bearing inputs and corresponding non-inverting combinatorial data-bearing inputs to said inverted logic outputs and said non-inverted logic outputs, wherein said precharge wave and/or said predischarge wave is encoded in data received on the inverting and non-inverting combinatorial data-bearing inputs.

7. A Divided Wave Dynamic Differential Logic DPA-resistant logic circuit, comprising:

a first logic tree comprising a plurality of first combinatorial data-bearing logic tree inputs and a plurality of first logic tree outputs and configured to, during an evaluation phase, receive inverted input data and corresponding non-inverted input data on said first combinatorial data-bearing logic tree inputs and to produce first output data on said first logic tree outputs; and

a dual of said first logic tree comprising a plurality of dual combinatorial data-bearing logic tree inputs and a plurality of dual logic tree outputs and configured to, during said evaluation phase, receive said inverted input data and said corresponding non-inverted input data on said dual combinatorial data-bearing logic tree inputs and produce inverted first output data on said dual logic tree outputs,

said first logic tree and said dual of said first logic tree further configured to, during a precharge and/or pre-discharge phase, receive a precharge wave and/or a pre-discharge wave on said first combinatorial data-bearing logic tree inputs and said dual combinatorial data-bearing logic tree inputs and propagate said precharge wave and/or pre-discharge wave to said first logic tree outputs and said dual logic tree outputs, wherein said precharge wave and/or said predischarge wave is encoded in data received on the first and dual combinatorial data-bearing inputs.